CENTRAL TEXAS COLLEGE
ELMT 2339
ADVANCED PROGRAMMABLE LOGIC CONTROLLERS

Semester Hours Credit: 3

INSTRUCTOR: ___________________________

OFFICE HOURS: _________________________

I. INTRODUCTION

A. Advanced applications of programmable logic controllers as used in industrial environments including concepts of programming, industrial applications, troubleshooting ladder logic, and interfacing of equipment.

B. This course is a requirement/recommended elective for …

C. Prerequisite: CETT-1425, CETT-1429 and ELMT-1301

II. LEARNING OUTCOMES

Upon successful completion of this course, the student will be able to:

A. Test designed Field Programmable Gate Array (FPGA) circuits (C8, C16)
B. Perform state machine design (F4, F10)
C. Interface analog and digital circuits (F12, C18, & C19)
D. Analyze logic gate circuitry (F8, F7, C16, & C19)
E. Use memory devices with FPGA’s (F11, F12, & C19)

III. INSTRUCTIONAL MATERIALS

A. The instructional materials identified for this course are viewable through www.ctcd.edu/books

B. Other Instructional Materials: None
IV. COURSE REQUIREMENTS

A. Reading Assignments: Chapter text as assigned. The student may be quizzed at end of each chapter.

B. Class Performance: Students are required to be in class on time. Excessive tardiness (four) will result in a five point reduction to the final grade. It is the recommendation of this department that students exchange telephone numbers so that they may acquire missed lecture notes and assignments.

C. Class Participation: Students are expected to be interactive with the instructor during lecture. A question/response format will be used. Class participation is part of the Lab Experiment grade and is based on the amount of participation each student contributes to the lab’s results.

V. EXAMINATIONS

There will be two exams, a Mid-Term and a Final Exam, each covering the chapters completed in class. A general review will be given before each exam. Should a test be missed due to extenuating circumstances, you may contact the instructor for a make-up exam. Make-up exams may have more questions than the normally scheduled test. In addition to the two exams, other exams or quizzes may be given at the discretion of the instructor.

VI. SEMESTER GRADE COMPUTATION

| Homework/Quizzes | 300 Points | 1000 – 900 = A |
| Exam One         | 200 Points | 899 - 800 = B  |
| Final Exam       | Pass/Fail  | 799 - 700 = C  |
| Lab Projects     | 500 Points | 699 - 600 = D  |
| **Total**        | 1000 Points| 599 - 0 = F    |

Students who do not complete all projects successfully, with approval by the instructor, will receive an Incomplete for the course grade and will have three weeks into the next semester to finish the projects or their grade will become an F.

VII. ATTENDANCE

Students are required to attend all classes in which they have enrolled. Students are required to be in the classrooms on time and remain for the duration of the class. Any time a student has 10 hours absence, an administrative withdrawal will be submitted.

A. Four Classes of 2 ½ hours = 10 Hours
B. Late for Class = 1 Hour Absence: 10 Times = 10 Hours
VIII. NOTES AND ADDITIONAL INSTRUCTIONS FROM THE INSTRUCTOR

A. **Course Withdrawal:** It is the student’s responsibility to officially withdraw from a course if circumstances prevent attendance. Any student who desires to, or must, officially withdraw from a course after the first scheduled class meeting, must file a Central Texas College Application of Withdrawal (CTC Form 59). The withdrawal form must be signed by the student.

A student who officially withdraws will be awarded the grade of W provided the student’s attendance and academic performance are satisfactory at the time of official withdrawal. Students must file a withdrawal application with the College before they may be considered for withdrawal. A student may not withdraw from a class for which the instructor has previously issued the student a grade of F.

B. **Administrative Withdrawal:** An administrative withdrawal may be initiated when the student fails to meet College attendance requirements.

C. **Incomplete Grade:** The College catalog states an incomplete grade may be given in those cases where the student has completed the majority of the course work, but because of personal illness, death in the immediate family, or military orders, the student is unable to complete the requirements for a course. Prior approval from the instructor is required before the grade of “IP” for Incomplete is recorded. A student who merely fails to show for the final examination will receive a zero for the final and an F for the course.

D. **Cellular Phones and Beepers:** Cellular phones and beepers will be turned off while the student is in the classroom or laboratory.

E. **Americans with Disabilities Act (ADA):** Disability Support Services provides services to students who have appropriate documentation of a disability. Students requiring accommodations for class are responsible for contacting the Office of Disability Support Services (DSS) located on the central campus. This service is available to all students, regardless of location. Explore the website at www.ctcd.edu/disability-support for further information. Reasonable accommodations will be given in accordance with the federal and state laws through the DSS office.

F. **Instructor Discretion:** The instructor reserves the right of final decision in course requirements.

G. ** Civility:** Individuals are expected to be cognizant of what a constructive educational experience is and respectful of those participating in a learning environment. Failure to do so can result in disciplinary action up to and including expulsion.
IX. COURSE OUTLINE

A. Lesson One: State Machine Design

1. **Lesson Objectives:** Upon successful completion of this lesson, the student will be able to:

   a. Describe the components of a state machine.
   b. Distinguish between Moore and Mealy implementations of state machines.
   c. Draw the state diagram of a state machine from a verbal description.
   d. Use the “classical” (state table) method of state machine design to determine the Boolean equations of the state machine.
   e. Translate the Boolean equations of a state machine into a Block Diagram File in Altera’s Quartus II software.
   f. Write VHDL code to implement state machines.
   g. Create simulations in Quartus II to verify the function of a state machine design.
   h. Determine whether the output of a state machine is vulnerable to asynchronous changes of input.
   i. Design state machine applications, such as a switch debouncer, a single-pulse generator, and a traffic light controller.

2. **Learning Activities:**
   a. Read Chapter 10 in the textbook.
   b. Complete assigned problems at end of chapter.
   c. Complete projects as assigned.

B. Lesson Two: Logic Gate Circuitry

1. **Lesson Objectives:** Upon successful completion of this lesson, the student will be able to:

   a. Name the various logic families most commonly in use today and state advantages and disadvantages of each.
   b. Define propagation delay.
   c. Calculate propagation delay of simple circuits, using datasheets.
   d. Define flip-flop timing parameters such as setup time, hold time, pulse width, recovery time, and propagation delay.
   e. Determine the values of flip-flop timing parameters from a device datasheet.
   f. Define fanout and calculate its value, using datasheets.
   g. Calculate power dissipation of TTL and CMOS circuits.
   h. Calculate noise margin of a logic gate from datasheets.
i. Draw circuits that will interface various CMOS and TTL gates.

j. Explain how a bipolar junction transistor can be used as a logic inverter.

k. Describe the function of a TTL input transistor in all possible input states: HIGH, LOW, and open-circuit.

l. Explain the operation of a totem pole output.

m. Illustrate how a totem pole output generates power line noise and describe how to remedy this problem.

n. Illustrate why totem pole outputs cannot be tied together.

o. Explain the difference between open-collector and totem pole outputs of a TTL gate.

p. Illustrate the operation of TTL open-collector inverter, NAND, and NOR gates.

q. Write the Boolean expression of a wired-AND circuit.

r. Design a circuit that uses an open-collector gate to drive a high-current load.

s. Calculate the value of a pull-up resistor at the output of an open-collector gate.

t. Explain the operation of a tristate gate and name several of its advantages.

u. Design a circuit using a tristate bus driver to direct the flow of data from one device to another.

v. Describe the basic structure of a MOSFET and state its bias voltage.

w. Draw the circuit of a CMOS inverter and show how it works.

x. Draw the circuits of CMOS NAND and NOR gates and explain the operation of each.

y. Design a circuit using a CMOS transmission gate to enable and inhibit digital and analog signals.

z. Interpret TTL datasheets to distinguish between the various TTL families.

aa. Describe the use of the Schottky barrier diode in TTL gates.

bb. Calculate speed-power products from datasheets.

2. Learning Activities:

   a. Read Chapter 11 of the textbook.

   b. Complete assigned problems at end of the chapter.

   c. Complete projects as assigned.

C. Lesson Three: Interfacing Analog and Digital Circuits

1. Lesson Objectives: Upon successful completion of this lesson, the student will be able to:
a. Define the terms “analog” and “digital” and give examples of each.

b. Explain the sampling of an analog signal and the effects of sampling frequency and quantization on the quality of the converted digital signal.

c. Describe the coding of data in analog-to-digital and digital-to-analog converters for unipolar, offset binary, and 2’s complement coding.

d. Perform calculations to convert input voltages to unipolar, offset binary, or 2’s complement codes in an analog-to-digital converter.

e. Perform calculations to determine output voltages of a digital-to-analog converter, given an input code in unipolar, offset binary, or 2’s complement format.

f. Draw the block diagram of a generic digital-to-analog converter (DAC) and circuits of a weighted resistor DAC and an R-2R ladder DAC.

g. Calculate analog output voltages of a DAC, given a reference voltage and a digital input code.

h. Configure an MC1408 integrated circuit DAC for unipolar and bipolar output, and calculate output voltage from known component values, reference voltage, and digital inputs.

i. Describe important performance specifications of a digital-to-analog converter.

j. Draw the circuit for a flash analog-to-digital converter (ADC) and briefly explain its operation.

k. Define “quantization error” and describe its effect on the output of an ADC.

l. Explain the basis of the successive approximation ADC, draw its block diagram, and briefly describe its operation.

m. Describe the operation of an integrator with constant input voltage.

n. Draw the block diagram of a dual slope (integrating) ADC and briefly explain its operation.

o. Draw the block diagram of a sigma-delta analog-to-digital converter, briefly explain its operation, and perform calculations to determine its output data stream.

p. Explain the necessity of a sample and hold circuit in an ADC and its operation.

q. State the Nyquist sampling theorem and do simple calculations of maximum analog frequencies that can be accurately sampled by an ADC system.

r. Describe the phenomenon of aliasing and explain how it arises and how it can be remedied.

s. Interface an ADC0808 analog-to-digital converter to a CPLD-based state machine.

T. Design a 4-channel data acquisition system, including an ADC0808 analog-to-digital converter and a CPLD-based state machine.
2. **Learning Activities:**

   a. Read Chapter 12 in the textbook.
   b. Complete assigned problems at end of the chapter.
   c. Complete projects as assigned.

D. **Lesson Four: Memory Devices and Systems**

1. **Lesson Objectives:** Upon successful completion of this lesson, the student will be able to:

   a. Describe basic memory concepts of address and data.
   b. Understand how latches and flip-flops act as simple memory devices and sketch simple memory systems based on these devices.
   c. Distinguish between random access read/write memory (RAM) and read-only memory (ROM).
   d. Describe the uses of tristate logic in data bussing.
   e. Sketch the circuits of static and dynamic RAM cells.
   f. Sketch a block diagram of a static or dynamic RAM chip.
   g. Describe various types of ROM cells and arrays: mask-programmed, UV erasable, and electrically erasable.
   h. Use various types of ROM in simple applications, such as digital function generation.
   i. Describe the basic configuration of flash memory.
   j. Describe the basic configuration and operation of two types of sequential memory: first-in-first-out (FIFO) and last-in-first-out (LIFO).
   k. Describe how dynamic RAM is configured into high-capacity memory modules.
   l. Sketch a basic memory system, consisting of several memory devices, an address and a data bus, and address decoding circuitry.
   m. Represent the location of various memory device addresses on a system memory map.
   n. Recognize and eliminate conditions leading to bus contention in a memory system.
   o. Expand memory capacity by parallel bussing and CPLD-based decoding.

2. **Learning Activities:**

   a. Read Chapter 13 in the textbook.
   b. Complete assigned problems at end of chapter.
   c. Complete projects as assigned.
E. Lesson Five: Introduction to Microprocessors

1. Lesson Objectives: Upon successful completion of this lesson, the student will be able to:
   a. Draw the block diagram of a simplified microcomputer system, showing blocks for the various components, interconnected by address, data, and control busses.
   b. Describe bus contention and what can be done to remedy this problem.
   c. Describe synchronous and asynchronous register data transfers and draw timing diagrams to represent them.
   d. Describe the functions of the registers in a model microcomputer system.
   e. Indicate the sequence of control signals required to fetch and execute an instruction in a model microcomputer system and represent the transfers on a timing diagram.
   f. Describe the functions of simple RISC instructions, such as LOAD, ADD, OUTPUT, and HALT.
   g. List the various functions of an 8-function ALU and analyze a VHDL file that implements these functions.
   h. Draw logic diagrams showing different methods of creating a tristate bus in an Altera CPLD. Write VHDL files to implement a tristate bus.
   i. Write VHDL files to implement the function of registers in a RISC CPU.
   j. Use the Quartus II Block Editor to create block diagrams with the blocks connected by conduit lines.
   k. Analyze VHDL files that implement registers and multiplexers for the RISC8v1.
   l. Create Memory Initialization Files to store program instructions and operands in the system ROM for a RISC microcomputer.
   m. Analyze the structure of a VHDL file that defines the function of the RISC8v1 controller.
   n. Modify the VHDL code for the controller to add new instructions to the RISC8v1 MCU.
   o. Describe the operation of a branch instruction and the hardware modifications required to implement it.

2. Learning Activities:
   a. Read Chapter 14 in the textbook.
   b. Complete assigned problems at end of chapter.
   c. Complete projects as assigned.